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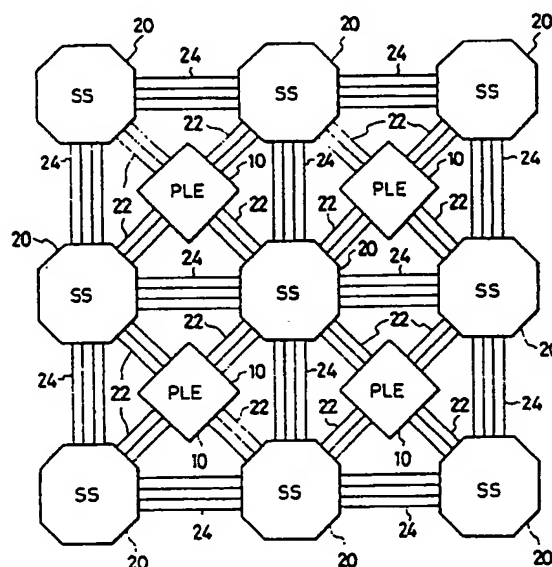
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(54) **Programmable logic device.**

(57) There is provided a programmable logic device (PLD) which includes a programmable wiring, the programmable wiring comprising: a plurality of switch stations (SS), first wirings (22) each for directly connecting some terminals among input/output terminals of said SSs to input/output terminals of adjacent programmable logic elements (PLE), and second wirings (24) each for directly connecting some terminals among the input/output terminals of said SSs to input/output terminals of the adjacent SS. Hereby, the numbers of involved switches, through which associated signals pass, can be reduced.

FIG. 1



EP 0 360 540 A2

Programmable logic device

The present invention relates to a programmable logic device which permits a user to electrically program an arbitrary logic circuit at his hand, and more specifically to an improved programmable logic device, which includes a highly functional programmable wiring of a reduced occupation area that comprises a plurality of programmable logic elements, the programmable logic elements being connected with each other through the programmable wiring.

There is conventionally known a programmable logic device (hereinafter simply referred to as a PLD), that is an integrated circuit with which a user can construct an arbitrary logic circuit at his hand.

The prior PLD primarily includes a programmable logic element (hereinafter simply referred to as a PLE) which is configurable to construct a user's own logic, a circuit function-defining memory cell for defining the logic function of the PLE and an interconnection relation among internal wirings, an programmable input/output block (hereinafter simply referred to as an IOB) for interfacing between external device packaging pins and an internal logic circuit (i.e. the PLE), and a programmable wiring for establishing a wiring path to connect input/output signals into/from the IOB and the PLE to a desired network

The programmable wiring is hitherto comprised, as illustrated for example in Fig. 9, of horizontal wirings 12 disposed between adjacent lines of the respective PLEs 10 (and IOBs) vertical wirings 14 disposed between adjacent columns of the respective PLEs 10 (and IOBs), switching matrixes 16 including interwiring switches 16A each disposed at intersections of the lines and the columns of the respective horizontal and vertical wirings 12 and 14 for interconnecting the wirings from the adjacent columns and lines, and input/output switches (hereinafter referred to as IOSs) 18 each disposed at position correspondingly to the adjacent PLEs 10 of the respective wirings 12 and 14 for connecting inputs and outputs into and from the adjacent PLEs 10 to the wirings 12 or 14.

The interwiring switches 16A and IOS 18 are controllable by each bit of circuit function-defining data, respectively, for establishing arbitrary wiring.

However, since in such a prior PLD, the IOSs 18 of the respective PLEs 10 and the interwiring switches 16A are independently provided, interconnection between the two PLEs 10 requires two, without fail, IOSs 18 and at least one switching matrix 18 although they are disposed far away or just adjacently, further requiring an increased number of the switches and complicated wiring, followed by a large occupation area of the PLD.

Additionally, there are required many gates or switches, through which associated signals pass, thereby attenuating the signals and lowering the reliability of the device.

In view of the drawbacks of the prior art, it is an object of the present invention to provide a PLD capable of optimizing a programmable wiring and of achieving the high function and reduced occupation area thereof.

In accordance with the present invention, there is provided a PLD including a plurality of programmable logic elements connected to each other through a programmable wiring, said programmable wiring comprising a plurality of switch stations each having a plurality of input/output terminals and each including therein switch elements for interconnecting said input/output terminals, first wirings each for directly connecting some terminals among said input/output terminals of said switch stations to input/output terminals of said adjacent logic elements, and second wirings each for directly connecting some terminals among said input/output terminals of said switch stations to the input/output terminals of the adjacent switch stations.

The present inventors have found in their investigation of many design examples that most part (over 60 %) of wirings among the PLEs interconnects the adjacent PLEs.

The present invention, which is based upon such investigations, facilitates interconnection between the adjacent PLEs to achieve its high function and its reduced occupation area.

In a primary aspect of the present invention, as illustrated in Fig. 1, the aforementioned programmable wiring comprises a plurality of switch stations (hereinafter simply referred to as SSs) 20, first wiring 22 located diagonally in the figure each for directly connecting some terminals among the input/output terminals of the SSs 20 to the adjacent PLEs 10, and second wirings 24 located vertically and horizontally in the figure for directly connecting some terminals among the input/output terminals of the SSs 20 to the adjacent SSs. Here, the PLE 10 may include the input/output terminals: A, Din, B, C, RD, W, Y, K, D, Z, CE and X, as illustrated in Fig. 2 for example. Likewise, the SS 20 may include the input/output terminals: Y, K, D, W1 - W4, Z, CE, X, S1 - S4, A, Din, B, E1 - E4, W, RD, C and N1 - N4, as illustrated in Fig. 3 for example.

Hereby, as illustrated in Fig. 4, the number of the switches, through which an associated signal passes, can be reduced by a fraction corresponding to the prior IOSs. In particular, the adjacent two PLEs 10 can be interconnected through the only

one SS 20.

Additionally, since the direction of a wiring, through which an associated signal is transmitted, connected to the SS 20 can be clarified to make clear a relationship between the input and output of the SS 20, there is no need of unnecessarily switching among the outputs of the SS 20, differing from the prior case. Thus, any wiring path, which is not in need of connection, can be made obvious, thereby optimizing the circuit to, in this respect, reduce the number of the switches.

Furthermore, if there are any equivalent PLE input/outputs, then they can be taken into consideration clearly, so that flexibility of the wiring is less reduced even when a circuit construction is adopted with a reduced number of the switches and with many restrictions.

In accordance with the present invention, as described above, there is no need of providing such an IOS as in the prior case and hence the number of the switches can be reduced, thereby allowing any wiring to be reduced, resulting in a high function. In particular, wiring between the adjacent PLEs can be overwhelmingly advantageous. In addition, the reduction of the number of the switches can realize the reduced occupation area of the device.

More specifically, if the direction of wiring would be changed between the first and second wirings, it might facilitate the discrimination therebetween.

The exact nature of this invention, as well as other objects and advantages thereof, will be readily apparent from consideration of the following specification relating to the accompanying drawings, in which like reference characters designate the same or similar parts throughout the figures thereof and wherein:

Fig. 1 is a block diagram illustrating the basic arrangement of a programmable logic device (PLD) according to the present invention;

Fig. 2 is a block diagram exemplarily illustrating input/output terminals of a programmable logic element (PLE) for use in the PLD of Fig. 1;

Fig. 3 is a block diagram exemplarily illustrating input/output terminals of a switch station (SS) for use in the PLD of Fig. 1;

Fig. 4 is a block diagram illustrating the function of the PLD according to the present invention;

Fig. 5 is a block diagram illustrating the construction of an embodiment of the PLD according to the present invention;

Fig. 6 is a block diagram illustrating the construction of a PLE for use in the embodiment;

Fig. 7 is a block diagram exemplarily illustrating a switch table of a switch station for use in the embodiment of Fig. 5;

Fig. 8 is a circuit diagram exemplarily illustrating a circuit of the switch station constructed on the basis of the switch table of Fig. 7; and

Fig. 9 is a block diagram exemplarily illustrating a prior PLD including a prior programmable wiring.

In what follows, a preferred embodiment according to the present invention will be described in detail with reference to the accompanying drawings.

As shown in Fig. 5, the embodiment provides a PLD which includes a plurality of PLEs 10 connected to each other through a programmable wiring. The programmable wiring comprises a plurality of SSs 20, each of which has a plurality of input/output terminals, X, W, Q, S1, S2, B, A, E, CK, C, N1 and N2 and includes a switch 20A as shown in Fig. 8, for interconnecting the input/output terminals to each other, first wirings 22 located diagonally in the figure for directly connecting some terminals X, Q, B, A, CK and C of the input/output terminals of the SS 20 to the adjacent PLEs 10, and second wirings 24 located horizontally and vertically in the figure for directly connecting remaining terminals W, S1, S2, E, N1 and N2 of the input/output terminals of the SS 20 to the adjacent SSs 20.

The PLE 10 may be a sequential circuit, which includes, as illustrated in Fig. 6, a combined logic circuit (e.g., an AND circuit) 10A, into which general purpose inputs A, B and C are inputted, and a flip-flop 10B for delaying a combined logic output X from the combined logic circuit 10A in response to a clock CK to generate an output Q.

The SS 20 may be one to realize a switch table such for example as that illustrated in Fig. 7. The SS 20 which realize such a switch table of Fig. 7, may be constructed, as illustrated in Fig. 8 for example, with many switch elements 20A.

In the present embodiment, an arbitrary sequential circuit can be assured by programming in proper a function in each PLE 10, which is a sequential circuit, as well as wiring in the SS 20.

In accordance with the present embodiment, the first wirings 22 have same directions (diagonal directions) of wiring and the second wirings 24 have same directions (up-down and right-left directions) of wiring different from the first wirings 22, thereby facilitating the discrimination of any wiring among the wirings.

Although in the above embodiment the PLE 10 was the sequential circuit including the combined logic circuit 10A and the flip-flop 10B, the PLE 10 may be constructed without limitation thereto.

Additionally, the switch table, which can be realized by the SS 20, and the practice thereof are also not limited to the present embodiment.

Although a certain preferred embodiment has

been shown and described, it should be understood that many changes and modifications may be made therein without departing from the scope of the appended claims.

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Claims

1. A programmable logic device including a plurality of programmable logic elements (10) connected to each other through a programmable wiring, said programmable wiring comprising:
plurality of switch stations (20) each having a plurality of input/output terminals, each switch station including therein switch elements (20A) each for interconnecting said input/output terminals;
first wirings (22) each for directly connecting some terminals among said input/output terminals of said switch stations (20) to input/output terminals of the adjacent logic elements (10); and
second wirings (24) each for directly connecting some terminals among said input/output terminals of said switch stations (20) to the input/output terminals of the adjacent switch stations.
2. A programmable logic device according to claim 1 wherein said first wirings (22) have same directions of wiring and said second wirings (24) have same directions of wiring different from said first wiring.
3. A programmable logic device according to claim 1 wherein said switch station (20) comprises many switch elements (20A) to realize a predetermined switch table.
4. A programmable logic device according to claim 1 wherein said programmable logic element (10) is a sequential circuit which comprises a combined logic circuit (10A), into which any general-purpose input is inputted, and a flip-flop (10B) for delaying a combined logical output from said combined logic circuit in response to a clock signal (CK) to generate a delayed output (Q).

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FIG. 1

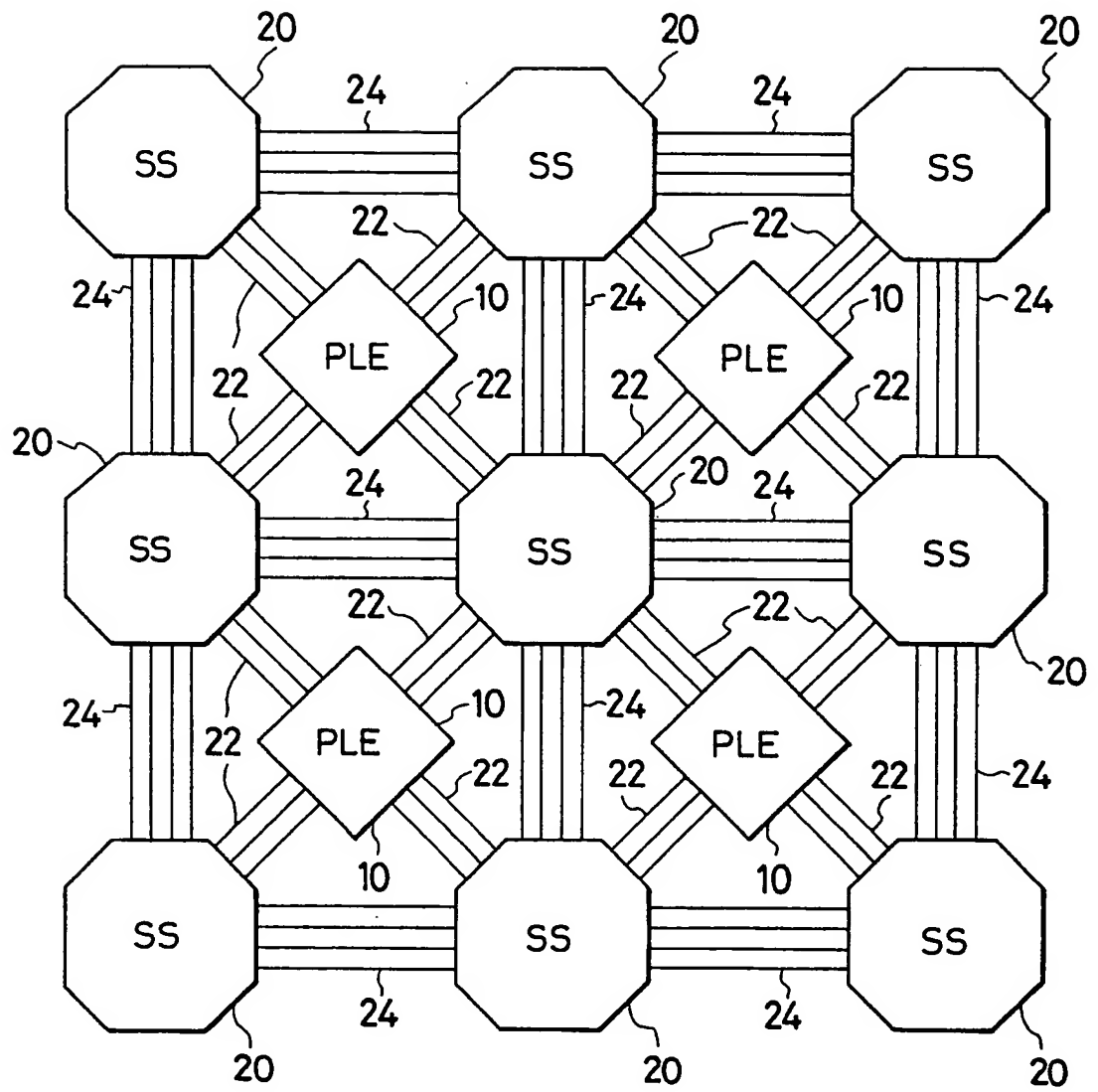


FIG.2

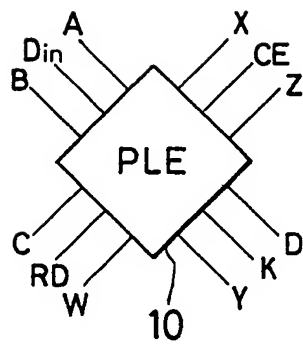


FIG.3

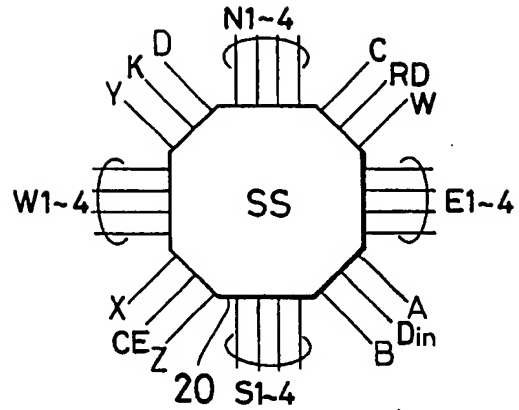


FIG.4

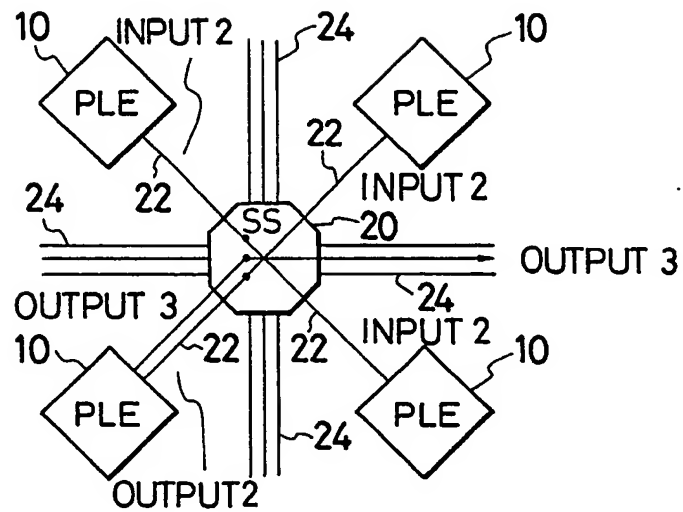


FIG. 5

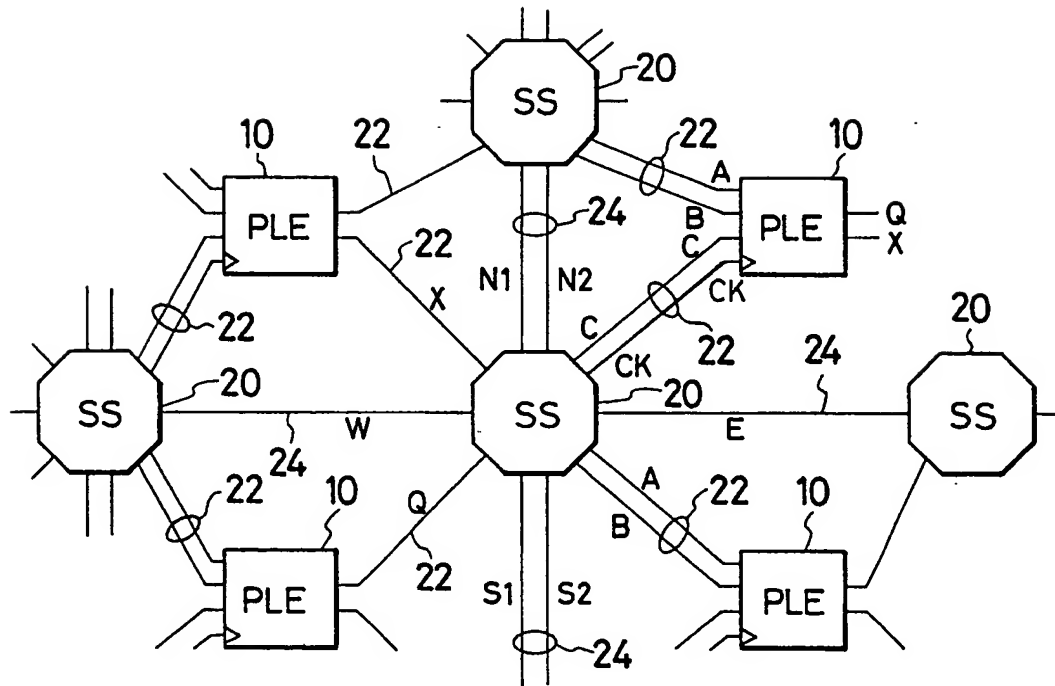


FIG. 6

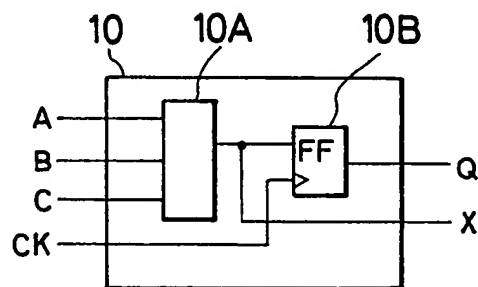
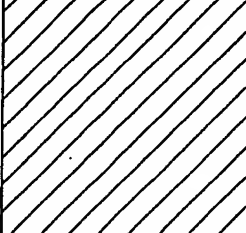
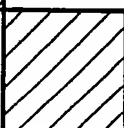
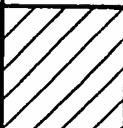
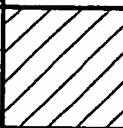
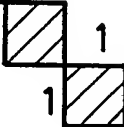


FIG. 7

| | A | B | C | CK | X | Q | N1 | N2 | S1 | S2 | W | E |
|----|---|---|---|----|--|---|--|----|---|----|---|---|
| A |  | | | | 1 | | 1 | | 1 | | 1 | |
| B | | | | | | 1 | | | | 1 | | 1 |
| C | | | | | 1 | 1 | | 1 | | 1 | 1 | 1 |
| CK | | | | | 1 | | | | | | 1 | 1 |
| X | 1 | | 1 | 1 |  | | 1 | | 1 | | 1 | 1 |
| Q | | 1 | 1 | | | | | 1 | | 1 | 1 | 1 |
| N1 | 1 | | | | 1 | |  | | 1 | | 1 | |
| N2 | | | 1 | | | 1 | | | | 1 | | 1 |
| S1 | 1 | | | | 1 | | 1 | |  | | 1 | |
| S2 | | 1 | 1 | | | 1 | | 1 | | | | 1 |
| W | 1 | | 1 | 1 | 1 | 1 | 1 | | 1 | |  | |
| E | | 1 | 1 | 1 | 1 | 1 | | 1 | | 1 | | |

1---WITH SWITCH

FIG. 8

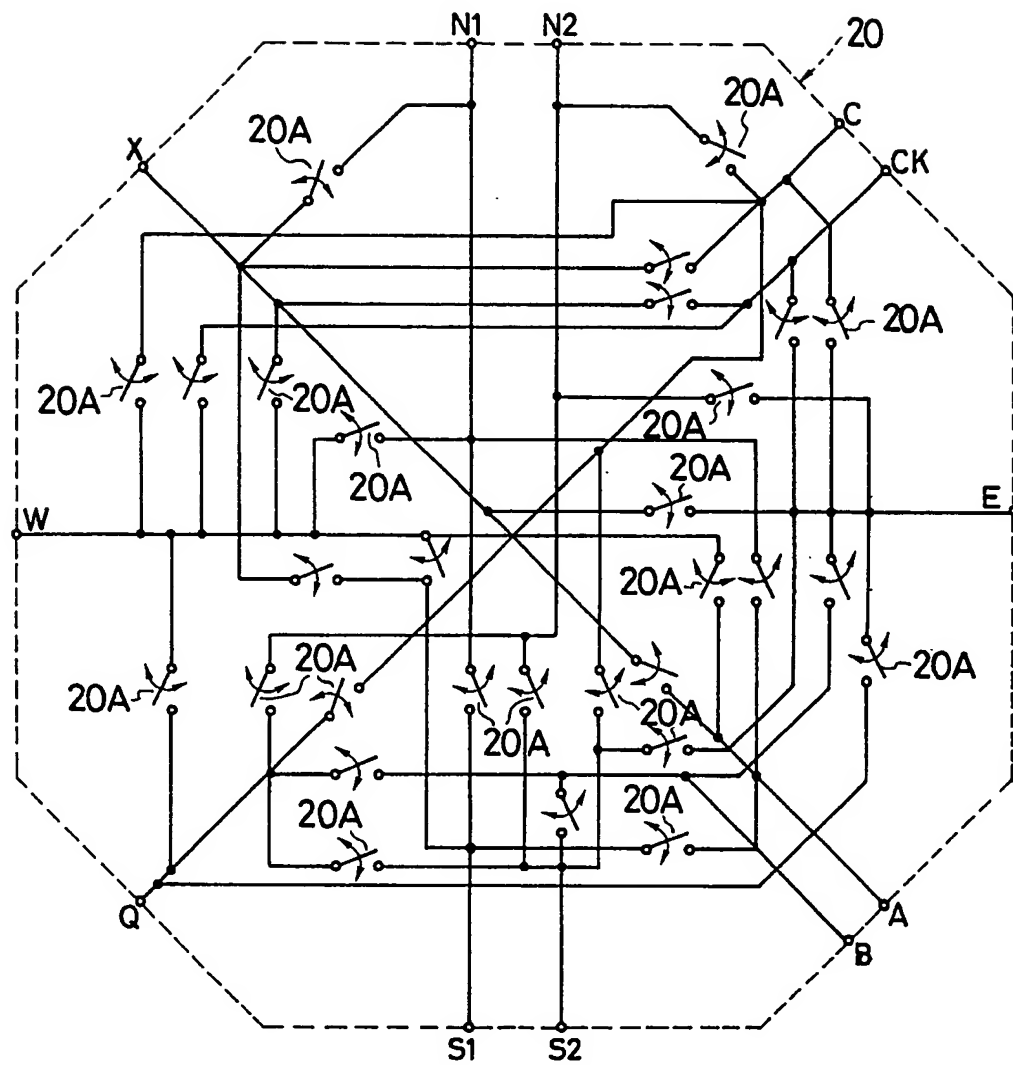


FIG. 9

